WHAT IS CLAIMED IS:

1. A method of fabricating a MOS transistor comprising:

a) forming an insulated gate pattern on a semiconductor substrate, the insulated gate pattern including a silicon pattern and a sacrificial layer pattern sequentially stacked;

b) forming spacers covering sidewalls of the gate pattern;

c) injecting impurity ions into the semiconductor substrate using the spacers and the gate pattern as ion injection masks to form source/drain regions;

d) removing the sacrificial layer pattern on the semiconductor substrate having the source/drain regions to expose the silicon pattern; and

e) converting the exposed silicon pattern into a gate silicide layer, and concurrently selectively forming source/drain silicide layers at surfaces of the source/drain regions.

2. The method of claim 1, wherein the semiconductor substrate is one of a single crystal silicon substrate, a silicon-on-insulator (SOI) substrate, and a strained silicon substrate.

3. The method of claim 1, wherein forming the insulated gate pattern comprises:

sequentially forming a gate insulating layer and a silicon layer on the semiconductor substrate;

forming a sacrificial layer on the semiconductor substrate having the silicon layer; and

sequentially patterning the sacrificial layer and the silicon layer.

4. The method of claim 3, further comprising doping the silicon layer with impurities to control a threshold voltage prior to formation of the sacrificial layer.

5. The method of claim 4, further comprising forming a buffer layer on top of the silicon layer before doping the silicon layer, wherein the buffer layer is etched to form a buffer layer pattern before patterning the silicon layer, and the buffer layer pattern is removed along with the sacrificial layer pattern to expose the silicon pattern.

6. The method of claim 4, wherein the impurities to control the threshold voltage are N-type.

7. The method of claim 4, wherein the impurities to control the threshold voltage are P-type.

8. The method of claim 3, further comprising doping the silicon layer on top of the semiconductor substrate with impurities to control a threshold voltage.

9. The method of claim 1, further comprising injecting impurity ions into the

semiconductor substrate using the gate pattern as an ion injection mask to form an LDD and a halo prior to formation of the spacers.

10. The method of claim 9, further comprising forming offset spacers covering the sidewalls of the gate pattern prior to formation of the LDD and the halo.

11. The method of claim 1, wherein the spacers are formed of an insulating layer having an etch selectivity with respect to the sacrificial layer pattern.

12. The method of claim 11, wherein the insulating layer having the etch selectivity is composed of multiple layers including a silicon oxide layer and a silicon nitride layer.

13. The method of claim 1, wherein converting the exposed silicon pattern into a gate silicide layer and concurrently forming source/drain silicide layers, comprises

forming a metal layer on the semiconductor substrate having the exposed silicon pattern;

annealing the metal layer until the exposed silicon pattern is silicided; and

removing the unreacted portion of the metal layer remaining on the spacers.

14. The method of claim 13, wherein the metal layer comprises at least one

metal layer comprising a metal selected from the group consisting of Ni, Co, W, and Ti.

15. The method of claim 13, wherein the metal layer comprises an alloy of a metal selected from the group consisting of Ni, Co, W, and Ti.

16. The method of claim 13, wherein the metal layer is one of a nickel layer and a nickel alloy layer.

17. The method of claim 1, further comprising forming a selective epitaxial growth layer on the source/drain regions before removing the sacrificial layer pattern.

18. A method of fabricating a CMOS transistor comprising:

a) defining an NMOS transistor region and a PMOS transistor region on a predetermined portion of a semiconductor substrate;

b) forming insulated gate patterns on the NMOS transistor region and the PMOS transistor region, each of the insulated gate patterns including a silicon pattern and a sacrificial layer pattern sequentially stacked;

c) forming spacers covering sidewalls of the gate patterns;

d) injecting impurity ions into the NMOS transistor region and the PMOS transistor region using the gate patterns and the spacers as ion injection masks to form source/drain regions;

e) removing the sacrificial layer patterns on the semiconductor substrate having the source/drain regions to expose the silicon patterns; and

f) converting the exposed silicon patterns into gate silicide layers, and concurrently selectively forming source/drain silicide layers at surfaces of the source/drain regions.

19. The method of claim 18, wherein the semiconductor substrate is one of a single crystal silicon substrate, a silicon-on-insulator (SOI) substrate, and a strained silicon substrate.

20. The method of claim 18, wherein the step of forming the gate patterns comprises:

sequentially forming a gate insulating layer and a silicon layer on the semiconductor substrate;

forming a sacrificial layer on the semiconductor substrate having the silicon layer; and

patterning the sacrificial layer and the silicon layer.

21. The method of claim 20, further comprising doping the silicon layer on the upper portion of the NMOS transistor region and the PMOS transistor region with impurities to control threshold voltages prior to formation of the sacrificial layer.

22. The method of claim 21, further comprising forming a buffer layer on

top of the silicon layer before doping the silicon layer, wherein the buffer layer is etched to form buffer layer patterns before patterning the silicon layer, and the buffer layer patterns are removed along with the sacrificial layer patterns in order to expose the silicon patterns.

23. The method of claim 21, wherein the impurities for doping the silicon layer on the upper portion of the NMOS transistor region and the PMOS transistor region to control the threshold voltages are N-type and P-type, respectively.

24. The method of claim 20, further comprising doping the silicon layer on the upper portion of the NMOS transistor region and the PMOS transistor region on the semiconductor substrate having the sacrificial layer with impurities to control threshold voltages.

25. The method of claim 18, further comprising injecting impurity ions into the NMOS transistor region and the PMOS transistor region on the semiconductor substrate using the gate patterns as an ion injection mask to form LDDs and halos prior to formation of the spacers.

26. The method of claim 25, further comprising forming offset spacers covering the sidewalls of the gate patterns prior to formation of the LDDs and the halos.

27. The method of claim 18, wherein the spacers are formed of an insulating layer having an etch selectivity with respect to the sacrificial layer patterns.

28. The method of claim 27, wherein the insulating layer having the etch selectivity is composed of multiple layers including a silicon oxide layer and a silicon nitride layer.

29. The method of claim 18, wherein converting the exposed silicon patterns into gate silicide layers and concurrently selectively forming source/drain silicide layers, comprises:

i) forming a metal layer on the semiconductor substrate having the exposed silicon patterns;

ii) annealing the metal layer until the exposed silicon patterns are silicided; and

iii) removing the unreacted portion of the metal layer remaining on the spacers.

30. The method of claim 29, wherein the metal layer is at least one metal layer comprising a metal selected from the group consisting of Ni, Co, W, and Ti.

31. The method of claim 29, wherein the metal layer comprises an alloy comprising a metal selected from the group consisting of Ni, Co, W, and Ti.

32. The method of claim 29, wherein the metal layer is a nickel layer or a nickel alloy layer.

33. The method of claim 18, further comprising forming a selective epitaxial growth layer on the source/drain regions before removing the sacrificial layer pattern.